REMARKS

This response responds to the Office Action dated December 9, 2005 in which the Examiner rejected claims 1-3 under 35 U.S.C. §103.

Claim 1 claims a semiconductor integrated circuit comprising a temperature detection circuit including a signal output circuit, a delay circuit, a logic circuit, a pulse width measurement circuit and a latch circuit. The signal output circuit outputs a first signal having at least one rising or falling portion. The delay circuit is connected to the signal output circuit and is formed of at least one inverter to output a delayed version of the first signal. The logic circuit receives the first signal and the delayed version of the first signal. The pulse width measurement circuit outputs a signal asserted in response to a signal directly received from the logic circuit having a pulse with a width of no less than a predetermined width corresponding to a temperature desired to be detected. The latch circuit latches a signal output from the pulse width measurement circuit. The pulse width measurement circuit has an integration circuit receiving a signal output from the logic circuit and a Schmitt trigger circuit receiving a signal output from the integration circuit. The Schmitt trigger circuit has a trigger potential set to have a value corresponding to the predetermined width.

Through the structure of the claimed invention having a delay circuit connected to a signal output circuit and having a pulse width measurement circuit directly receive a signal from a logic circuit as claimed in claim 1, the claimed invention provides a semiconductor integrated device that has a simple configuration in order to detect temperature. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-3 were rejected under 35 U.S.C. §103 as being unpatentable over *Ebihara et al.* (U.S. Patent No. 4,237,420) in view of *Mehnert* (U.S. Patent No. 4,873,518) and *Nishigaki* (JP 7-326714).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to claims and allows the claims to issue.

Ebihara et al appears to disclose a circuit for measuring temperature changes by means of an monostable multivibrator having a time constant element such as a resistor or capacitor which has a linear response to temperature variations. (col. 1, lines 4-8) FIG. 1 is a circuit diagram of such a conventional type of temperature sensing circuit. Numeral 10 indicates a temperature sensor circuit utilizing an OSM as a temperature sensor. The OSM consists of a two-input NOR gate 12, the output of which is connected to one terminal of a capacitor 16. One end of an adjustable resistor 14 is connected to one side of a power source, designated as Vdd, while the other terminal of resistor 14 is connected to the other terminal of capacitor 16 and to the input terminal of an inverter 18. The output of inverter 18 is connected back to one input of NOR gate 12, and to one input terminal of AND gate 24 of a pulse width measurement circuit 23. The other input terminal of two-input AND gate 24 is connected to a source of clock pulses Cx. The output of AND gate 24 is applied to the clock terminal of a counter circuit 26. Counter circuit 26 is reset by a signal Rx applied to its reset terminal prior to a temperature sensing operation being initiated. The count held in counter 26 is output in digital form, as output OD. (col. 2, lines 7-27)

Applicants respectfully traverse the Examiner's characterization of *Ebihara et al.* as showing a delay circuit OSM 10, logic circuit OSM 10 and pulse width measurement circuit. First, the Examiner characterizes the delay circuit in *Ebihara et al.* as being formed by only capacitor 16, variable resistor 14 and inverter 18. However, as clearly shown in Figure 1 of *Ebihara et al.* as well as described in column 2, lines 3-67, NOR gate 12 is part of the OSM 10. Thus, signal a output from start signal source 22 is input into NOR gate 12 of OSM 10. In other words, *Ebihara* et al. merely discloses an inverter 18 having its input connected to adjustable resister 14. Nothing in *Ebihara et al.* shows, teaches or suggests a delay circuit connected to a signal output circuit outputting a first signal as claimed in claim 1. Rather, the delay circuit 16, 14, 18 identified by the Examiner has a signal input through NOR gate 12.

Furthermore, Applicants respectfully traverse the Examiner's characterization of the logic circuit. The Examiner stated that OSM 10, including NOR gate 12, is also the logic circuit. However, as discussed above, NOR gate 12 is part of OSM 10. Based upon the Examiner's characterization, the delay circuit and logic circuit are the same circuit.

Also, Applicants respectfully traverse the Examiner's characterization of the logic circuit and pulse width measurement circuit. The Examiner characterizes the pulse width measurement circuit 23 as having a signal directly received from the logic circuit. However, the Examiner characterizes capacitor 16, variable resistor 14 and inverter 18 of the temperature sensor OSM 10 is being the delay circuit. The Examiner states that the signal output from the logic circuit (which is in fact NOR gate 12) is directly received from the logic circuit. As clearly shown in Figure 1, the

output from NOR gate 12 is input to the delay circuit 16, 14, 18 (as characterized by the Examiner) and is **not** directly received by the pulse width measurement circuit 23. In other words, *Ebihara et al.* merely discloses a pulse width measurement circuit 23 connected to the output of inverter 18 (delay circuit as characterized by the Examiner). Thus nothing in *Ebihara et al.* shows, teaches or suggests a pulse width measurement circuit directly receiving a signal from a logic circuit (NOR gate 12) as claimed in claim 1.

Finally, *Ebihara et al.* merely discloses that pulse width measurement circuit 23 includes an AND gate 24 and a counter circuit 26. Nothing in *Ebihara et al.* shows, teaches or suggests a pulse width measurement circuit having an integration circuit receiving a signal output from the logic circuit and a Schmitt trigger circuit as claimed in claim 1. Rather, *Ebihara et al.* merely discloses a pulse width measurement circuit 23 including an AND gate 24 and a counter circuit 26.

Mehnert appears to disclose a pulse width discriminator illustrated in FIG. 3, in like manner as the example of embodiment of FIG. 2, comprises the three D-flip-flops 45, 46 and 47, the three OR-gates 48, 49 and 50, the three AND-gates 52, 53 and 54 and the delay member 51, which are connected one with the other and function in like manner as was described in connection with FIG. 2. The most significant difference between both these examples of embodiment consists in that in the embodiment according to FIG. 3, the upper and lower limits are defined not in digital manner, but with the aid of analog circuits 60 to 65. Since all these analog circuits are built up in the same manner, their build-up and their function is described in the following only with reference to circuit 60. Circuit 60 possesses an RC-member, which is formed by a charging resistor 66 and a charging capacitor 67, as

time-determining member. Both these elements are connected each in series with the other and that terminal of the charging resistor 66, which forms one end of this series connection, is connected with a line 68, on which appear the input pulses, inverted by an inverter 69, of the pulse width discriminator 20. That terminal of the capacitor 67, which forms the other end of the RC-member 66 and 67, is applied to ground. Connected with the junction between the charging resistor 66 and the capacitor 67 is the input of a Schmitt trigger circuit 70, the output of which in the case of the analog switching circuits 60, 62 and 64 generate the lower limit signals driving the clock input of the associated D-flip-flop 45, 46 or 47 respectively and in the case of the analog circuit 61, 63 and 65 generates the upper limit signals driving the second input of the OR-gate 48, 49 and 50 and by way of its output the resetting input of the associated D-flip-flop. (col. 9, line 50 through col. 10, line 17)

Thus, *Mehnert* merely discloses a pulse width discriminator including a circuit 60 possessing a charging resistor 66 and a charging capacitor 67 and a Schmitt trigger circuit 70. Nothing in *Mehnert* shows, teaches or suggests a) a delay circuit connected to a signal output circuit or b) a pulse width measurement circuit directly receiving a signal from a logic circuit. Rather, *Mehnert* merely discloses a pulse width discriminator 20 receiving an output from an inverting Schmitt trigger circuit 18.

Nishigaki appears to disclose a device for measuring a chip's internal temperature including a buffer circuit 50 and a delay is utilized to measure the chip's internal temperature.

Thus, nothing in *Nishigaki* shows, teaches or suggests a) a delay circuit connected to a signal output circuit and b) a pulse width measurement circuit directly receiving a signal from a logic circuit as claimed in claim 1.

The combination of *Ebihara et al.*, *Mehnert* and *Nishigaki* would merely suggest to replace the pulse width measurement circuit 23 of *Ebihara et al.* with the pulse width discriminator 20 of *Mehnert* in a semiconductor device as taught by *Nishigaki*. Thus nothing in the combination of the references shows, teaches or suggests the structural interconnection of the elements as claimed in claim 1. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claims 2-3 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 would not have been obvious within the meaning of 35 U.S.C. §103 over *Ebihara et al, Mehnert* and *Nishigaki* at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicants respectfully request the Examiner enters this response for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time.

The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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